CLAIMS

1. An integrated circuit chip comprising:

a first interconnect metal layer;

a first intermetallic dielectric layer situated over said first interconnect metal layer;

a metal resistor situated over said first intermetallic dielectric layer and below a second intermetallic dielectric layer;

a second interconnect metal layer over said second intermetallic dielectric layer;

a first intermediate via connected to a first terminal of said metal resistor, said first intermediate via being further connected to a first metal segment patterned in said second interconnect metal layer;

a second intermediate via connected to a second terminal of said metal resistor, said second intermediate via being further connected to a second metal segment patterned in said second interconnect metal layer.

2. The integrated circuit chip of claim 1 wherein said metal resistor is selected from the group consisting of titanium nitride and tantalum nitride.

3. The integrated circuit chip of claim 1 wherein said first interconnect metal layer comprises aluminum.

4. The integrated circuit chip of claim 1 wherein said first intermetallic dielectric layer comprises HDPCVD silicon dioxide.

5. The integrated circuit chip of claim 1 wherein said second intermetallic dielectric layer comprises undoped silica glass.

6. The integrated circuit chip of claim 1 further comprising a dielectric cap layer situated between said metal resistor and said second intermetallic dielectric layer.

7. The integrated circuit chip of claim 6 wherein said dielectric cap layer comprises silicon nitride.

8. The integrated circuit chip of claim 1 further comprising an oxide cap layer situated between said metal resistor and said first intermetallic dielectric layer.

9. The integrated circuit chip of claim 8 wherein said oxide cap layer comprises PECVD silicon dioxide.

10. An integrated circuit chip comprising:

a first interconnect metal layer;

a first intermetallic dielectric layer situated over said first interconnect metal layer;

a metal resistor situated over said first intermetallic dielectric layer and below a second intermetallic dielectric layer;

a second interconnect metal layer over said second intermetallic dielectric layer;

a first intermediate via connected to a first terminal of said metal resistor, said first intermediate via being further connected to a first metal segment patterned in said first interconnect metal layer;

a second intermediate via connected to a second terminal of said metal resistor, said second intermediate via being further connected to a second metal segment patterned in said first interconnect metal layer.

11. The integrated circuit chip of claim 10 wherein said metal resistor is selected from the group consisting of titanium nitride and tantalum nitride.

12. The integrated circuit chip of claim 10 wherein said first intermetallic dielectric layer comprises HDPCVD silicon dioxide.

13. The integrated circuit chip of claim 10 wherein said second intermetallic dielectric layer comprises undoped silica glass.

14. The integrated circuit chip of claim 10 further comprising a dielectric cap layer situated between said metal resistor and said second intermetallic dielectric layer.

15. The integrated circuit chip of claim 14 wherein said dielectric cap layer comprises silicon nitride.

16. The integrated circuit chip of claim 10 wherein said first interconnect metal layer comprises aluminum.

17. The integrated circuit chip of claim 10 further comprising an oxide cap layer situated between said metal resistor and said first intermetallic dielectric layer.

18. The integrated circuit chip of claim 17 wherein said oxide cap layer comprises PECVD silicon dioxide.

19. A method for fabricating an integrated circuit chip, said method comprising steps of:

fabricating a first interconnect metal layer in said integrated circuit chip;

depositing a first intermetallic dielectric layer on said first interconnect metal layer;

depositing a resistor metal layer on said first intermetallic dielectric layer;

forming a metal resistor in said resistor metal layer;

depositing a second intermetallic dielectric layer on said metal resistor;

fabricating a second interconnect metal layer on said second intermetallic dielectric layer;

patterning a first metal segment and a second metal segment in said second interconnect metal layer;

etching a first intermediate via in said second intermetallic dielectric layer, said

first intermediate via connecting a first terminal of said metal resistor to said first metal segment in said second interconnect metal layer;

etching a second intermediate via in said second intermetallic dielectric layer, said second intermediate via connecting a second terminal of said metal resistor to said second metal segment in said second interconnect metal layer.

20. The method of claim 19 wherein said metal resistor is selected from the group consisting of titanium nitride and tantalum nitride.

21. The method of claim 19 wherein said first intermetallic dielectric layer comprises HDPCVD silicon dioxide.

22. The method of claim 19 wherein said second intermetallic dielectric layer comprises undoped silica glass.

23. The method of claim 19 further comprising a step of depositing a dielectric cap layer over said metal resistor after said forming step.

24. The method of claim 23 wherein said dielectric cap layer comprises silicon nitride.

25. The method of claim 19 further comprising a step of depositing an oxide

cap layer on said first intermetallic dielectric layer.

26. The method of claim 25 wherein said oxide cap layer comprises PECVD silicon dioxide.

27. The method of claim 19 wherein said first interconnect metal layer comprises aluminum.